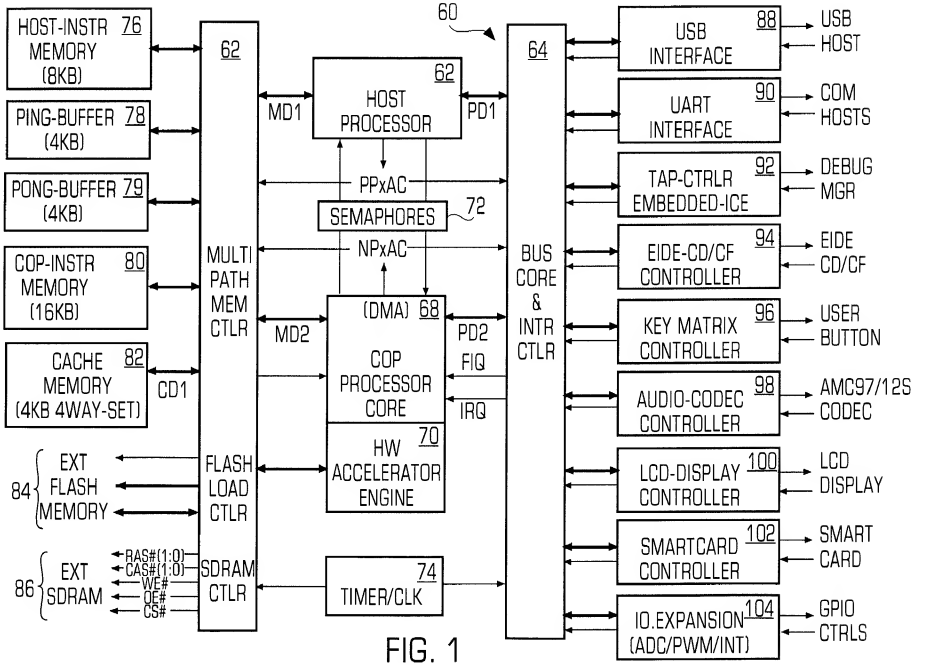


FIG. 1

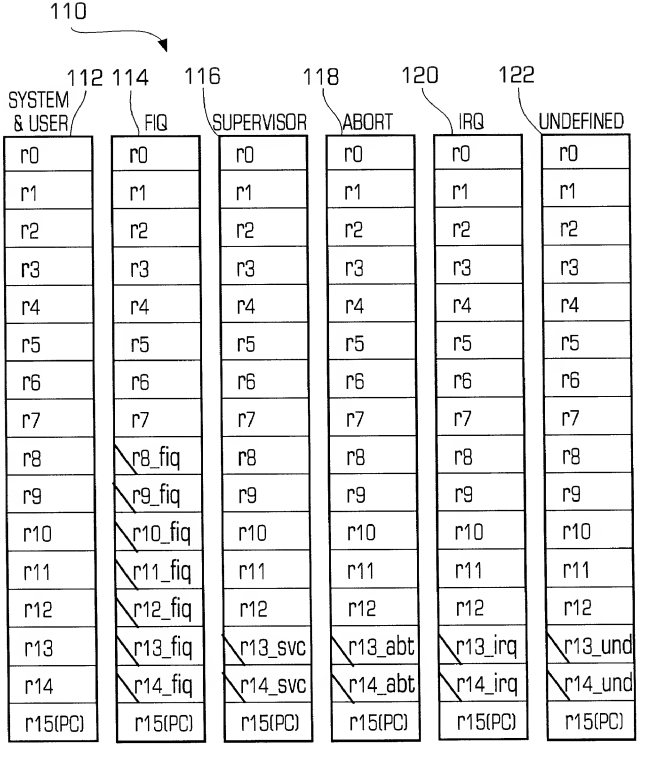

110
112
114
116
118
120
122
SYSTEM & USER
FIQ
SUPERVISOR
ABORT
IRQ
UNDEFINED
r0
r1
r2
r3
r4
r5
r6
r7
r8
r9
r10
r11
r12
r13
r14
r15(PC)
r8_fiq
r9_fiq
r10_fiq
r11_fiq
r12_fiq
r13_fiq
r14_fiq
r13_svc
r14_svc
r13_abt
r14_abt
r13_irq
r14_irq
r13_und
r14_und

FIG. 2

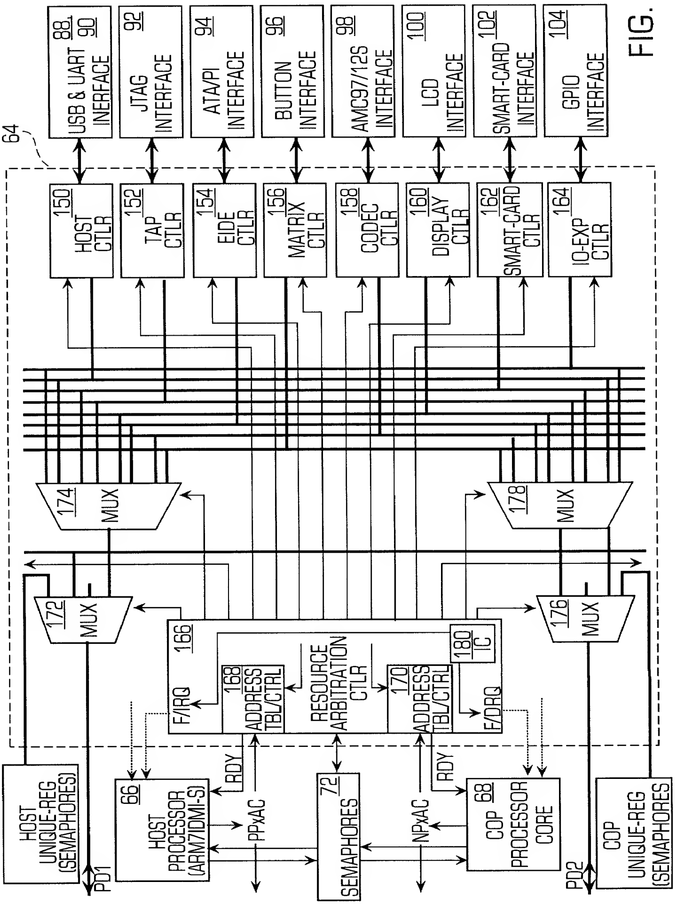

64
USB & UART INERFACE 88 90
JTAG INTERFACE 92
ATA/PI INTERFACE 94
BUTTON INTERFACE 96
AMC97/12S INTERFACE 98
LCD INTERFACE 100
SMART-CARD INTERFACE 102
GPIO INTERFACE 104
150 HOST CTLR
152 TAP CTLR
154 EIDE CTLR
156 MATRIX CTLR
158 CODEC CTLR
160 DISPLAY CTLR
162 SMART-CARD CTLR
164 IO-EXP CTLR
174 MUX
178 MUX
172 MUX
176 MUX
166
F/IRQ
168 ADDRESS TBL/CTRL
RESOURCE ARBITRATION CTLR
170 ADDRESS TBL/CTRL
180 IC
F/DRQ
HOST UNIQUE-REG (SEMAPHORES)
66 HOST PROCESSOR (ARM7IDMI-S)
RDY
PPxAC
72 SEMAPHORES
NPxAC
RDY
68 COP PROCESSOR CORE
COP UNIQUE-REG (SEMAPHORES)
PD1
PD2

FIG. 3

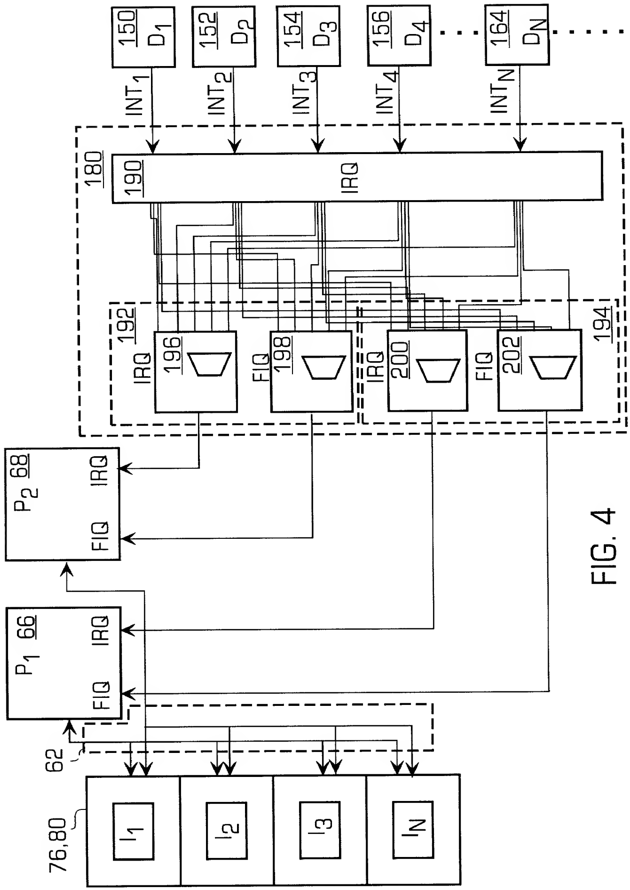
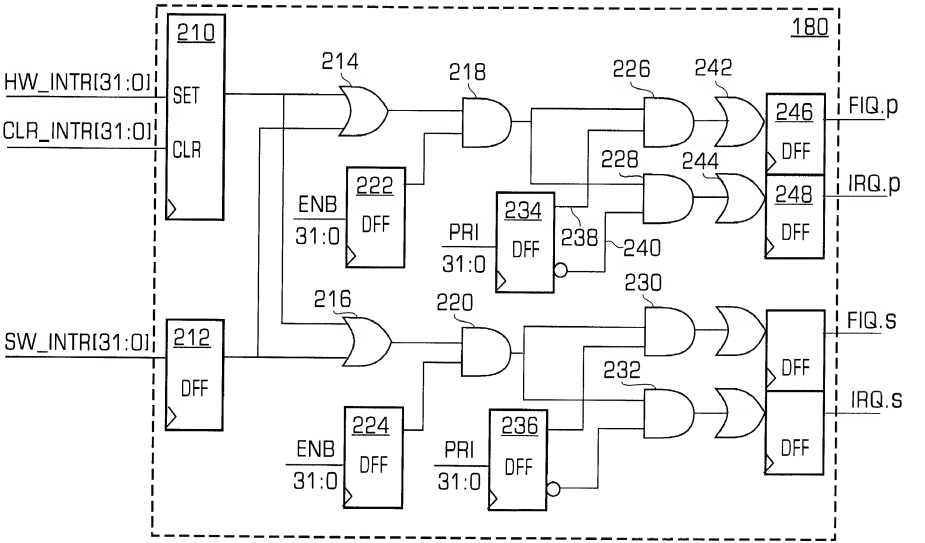

150
D1
152
D2
154
D3
156
D4
164
DN
INT1
INT2
INT3
INT4
INTN
180
190
IRQ
192
194
IRQ
196
FIQ
198
IRQ
200
FIQ
202
P2 68
IRQ
FIQ
P1 66
IRQ
FIQ
62
76,80
I1
I2
I3
IN

FIG. 4



FUNCTIONAL BLOCK DIAGRAM OF INTERRUPT CONTROLLER

FIG. 5

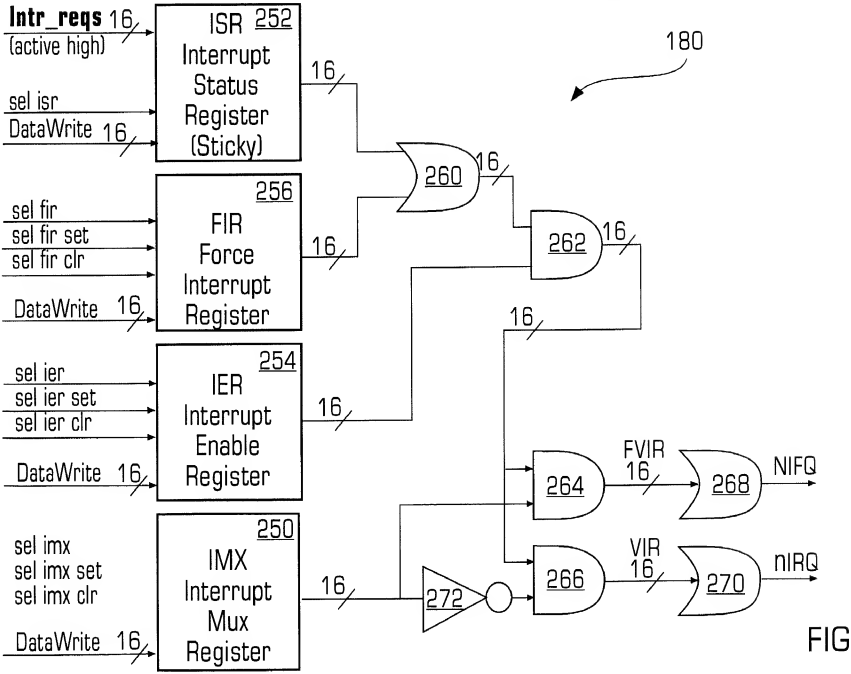

Intr_reqs 16
(active high)
sel isr
DataWrite 16
ISR 252
Interrupt
Status
Register
(Sticky)
16
180
260
16
262
16
16
sel fir
sel fir set
sel fir clr
DataWrite 16
256
FIR
Force
Interrupt
Register
16
sel ier
sel ier set
sel ier clr
DataWrite 16
254
IER
Interrupt
Enable
Register
16
sel imx
sel imx set
sel imx clr
DataWrite 16
250
IMX
Interrupt
Mux
Register
16
272
264
266
FVIR
16
VIR
16
268
270
NIFQ
nIRQ

FIG. 6

280

Offset	Register	Description
0	ISR	Interrupt Status Register
4	IER	Interrupt Enable Register
8	IER_set	Each bit written as one will set the corresponding bit in IER
C	IER_clr	Each bit written as one will clr the corresponding bit in IER
10	FIR	Force Interrupt Register
14	FIR_set	Each bit written as one will set the corresponding bit in FIR
18	FIR_clr	Each bit written as one will clr the corresponding bit in FIR
1C	IMX	Interrupt Mux Register ('1/0' Routes interrupt to nFIQ/nIRQ
20	IMX_set	Each bit written as one will set the corresponding bit in IMX
24	IMX_clr	Each bit written as one will clr the corresponding bit in IMX
28	VIR	Read only Valid Interrupt Register for nIRQ
2C	FVIR	Read only Fast Valid Interrupt Register for nFIQ

282

284

FIG. 7

Bit	Description
0	USB
1	UART A
2	UART B
3	External
4	USB Fast
5	Not Defined (CIF)
6	Not Defined
7	Not Defined (Keyboard)
8	EIDE 1
9	EIDE 2
A	Not Defined
B	Not Defined
C	Not Defined
D	Timer 2
E	Timer 1
F	Not defined
10	USB Reset
11	AC
12	Timer 1
13	Timer 2
31:14	Not Defined

FIG. 8

INTERRUPT CONTROLLER								
VIRQ_CPU	CF00:1000	RO	32B	VALID INTERRUPT STATUS FOR CPU (PRIMARY)	00000000			
VIRQ_COP	CF00:1004	RO	32B	VALID INTERRUPT STATUS FOR COP (SECONDARY)	00000000			
VFIQ_CPU	CF00:1008	RO	32B	FIQ VALID INTERRUPT STATUS FOR CPU (PRIMARY)	00000000			
VFIQ_COP	CF00:100C	RO	32B	FIQ VALID INTERRUPT STATUS FOR COP (SECONDARY)	00000000			
ISR (READ-ONLY)	CF00:1010	RO	32B	LATCHED INTERRUPT STATUS REGISTER (HW)	00000000			
FIR (READ-ONLY)	CF00:1014	RO	32B	FORCED INTERRUPT STATUS REGISTER (SW)	00000000			
FIR_SET	CF00:1018	SET	32B	FORCE INTERRUPT REGISTER SET	00000000			
FIR_CLR	CF00:101C	CLR	32B	FORCE INTERRUPT REGISTER CLEAR	00000000			
CPU_IER (READ-ONLY)	CF00:1020	RO	32B	ENABLED INTERRUPT SOURCE FOR CPU	00000000			
CPU_IER _SET	CF00:1024	SET	32B	SET INTERRUPT SOURCE FOR CPU	00000000			
CPU_IER _CLR	CF00:1028	CLR	32B	CLEAR INTERRUPT SOURCE FOR CPU	00000000			
CPU_IEP _CLASS	CF00:102C	RW	32B	CPU'S INTERRUPT ENABLE PRIORITY CLASS (FIQ/IRQ)	00000000			
COP_IER (READ-ONLY)	CF00:1030	RO	32B	ENABLED INTERRUPT SOURCE FOR COP	00000000			
COP_IER _SET	CF00:1034	SET	32B	SET INTERRUPT SOURCE FOR COP	00000000			
COP_IER _CLR	CF00:1038	CLR	32B	CLEAR INTERRUPT SOURCE FOR COP	00000000			
COP_IEP _CLASS	CF00:103C	RW	32B	COP'S INTERRUPT ENABLE PRIORITY CLASS (FIQ/IRQ)	00000000			
DMA_STATUS	CF00:1040	RO	32B	DMA INTERRUPT SOURCE STATUS	00000000			

FIG. 9A

IRQ31	IRQ30	IRQ29	IRQ28	IRQ27	IRQ26	IRQ25	IRQ24	IRQ23	IRQ22	IRQ21	IRQ20	IRQ19	IRQ18	IRQ17	IRQ16
IRQ31	IRQ30	IRQ29	IRQ28	IRQ27	IRQ26	IRQ25	IRQ24	IRQ23	IRQ22	IRQ21	IRQ20	IRQ19	IRQ18	IRQ17	IRQ16
FIQ31	FIQ30	FIQ29	FIQ28	FIQ27	FIQ26	FIQ25	FIQ24	FIQ23	FIQ22	FIQ21	FIQ20	FIQ19	FIQ18	FIQ17	FIQ16
FIQ31	FIQ30	FIQ29	FIQ28	FIQ27	FIQ26	FIQ25	FIQ24	FIQ23	FIQ22	FIQ21	FIQ20	FIQ19	FIQ18	FIQ17	FIQ16
ISR31	ISR30	ISR29	ISR28	ISR27	ISR26	ISR25	ISR24	ISR23	ISR22	ISR21	ISR20	ISR19	ISR18	ISR17	ISR16
FIR31	FIR30	FIR29	FIR28	FIR27	FIR26	FIR25	FIR24	FIR23	FIR22	FIR21	FIR20	FIR19	FIR18	FIR17	FIR16
IER31	IER30	IER29	IER28	IER27	IER26	IER25	IER24	IER23	IER22	IER21	IER20	IER19	IER18	IER17	IER16
IER31	IER30	IER29	IER28	IER27	IER26	IER25	IER24	IER23	IER22	IER21	IER20	IER19	IER18	IER17	IER16

FIG. 9B

IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
FIQ15	FIQ14	FIQ13	FIQ12	FIQ11	FIQ10	FIQ9	FIQ8	FIQ7	FIQ6	FIQ5	FIQ4	FIQ3	FIQ2	FIQ1	FIQ0
FIQ15	FIQ14	FIQ13	FIQ12	FIQ11	FIQ10	FIQ9	FIQ8	FIQ7	FIQ6	FIQ5	FIQ4	FIQ3	FIQ2	FIQ1	FIQ0
ISR15	ISR14	ISR13	ISR12	ISR11	ISR10	ISR9	ISR8	ISR7	ISR6	ISR5	ISR4	ISR3	ISR2	ISR1	ISR0
FIR15	FIR14	FIR13	FIR12	FIR11	FIR10	FIR9	FIR8	FIR7	FIR6	FIR5	FIR4	FIR3	FIR2	FIR1	FIR0
FIR_SET (SET FORCED INTERRUPT BIT)															
FIR_CLR (CLEAR FORCED INTERRUPT BIT)															
IER15	IER14	IER13	IER12	IER11	IER10	IER9	IER8	IER7	IER6	IER5	IER4	IER3	IER2	IER1	IER0
CPU_IER_SET (ENABLE INTERRUPT SOURCE FOR CPU)															
CPU_IER_CLR (DISABLE INTERRUPT SOURCE FOR CPU)															
CPU-IEP_CLASS (SET PRIORITY INTERRUPT SOURCE FOR CPU)															
IER15	IER14	IER13	IER12	IER11	IER10	IER9	IER8	IER7	IER6	IER5	IER4	IER3	IER2	IER1	IER0
COP_IER_SET (ENABLE INTERRUPT SOURCE FOR COP)															
COP_IER_CLR (DISABLE INTERRUPT SOURCE FOR COP)															
COP_IEP_CLASS (SET PRIORITY INTERRUPT SOURCE FOR COP)															
DMA_SOURCE_STATUS															

FIG. 9C